

# Optimization for Embedded Systems Platforms

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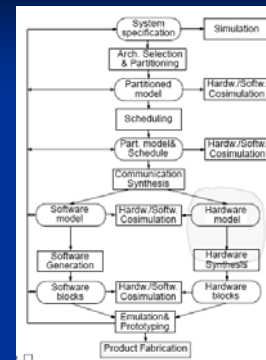
## Embedded Systems

- **Complexity:** new computer aided methodologies are needed in the context of increasing complexity (SoC).
- **Verification:** starting from a (formal) system specification which is validated, and performing well defined design steps (transformations) with verifiable outputs.
- **Time to market:** only efficient tools and reuse can bring design productivity up to the expected level.

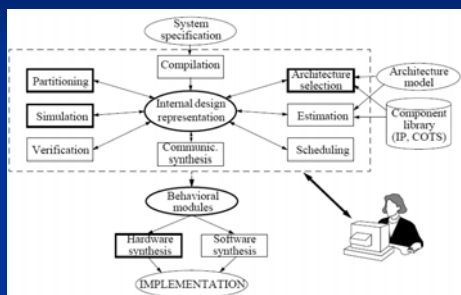
## System Synthesis

- **Input:** an implementation independent specification of the system; this includes: functionality and constraints.
- **The synthesis tasks:**
  - To select the architecture;
  - To partition functionality over the components of the architecture;
  - To schedule activities
  - To generate behavioral modules corresponding to the hardware and software domain of the implementation, including interface modules.
  - The behavioral modules resulted from the previous steps are further synthesized into the actual hardware and/or software implementation.

## System Synthesis



## System Synthesis



## Synthesis Steps

- **Synthesis:**
  - Transformation of a representation in the behavioral domain to a representation of the same design in the structural domain (at the same abstraction level).
  - The structural description which results after a synthesis step is formulated as an interconnection of abstract components.
  - Each such component is functionally specified at the following, lower abstraction level. These functional specifications are the input for the following synthesis step.

## Synthesis Steps

- **System synthesis**
  - Input: System level specification (interacting processes) + design constraints
  - Output: Behavioral elements to be synthesised to hardware and software + System architecture + Process schedule and mapping
- **High level (behavioral) synthesis**
  - Input: Algorithmic description
  - Output: RT level description of the controller (FSM) + net-list (data path)

## Synthesis Steps

- **RT level synthesis**
  - Input: RT level description of the controller (FSM) + net-list
  - Output: Blocks of combinational and memory elements
- **Logic synthesis**
  - Input: Blocks of combinational and memory elements (as boolean functions)
  - Output: gate-level net-list
- **Physical design**
  - Input: gate-level netlist
  - Output: geometrical layout for a given technology